Claims

[c1] 1. A dynamic semiconductor memory device performing a refresh operation in a standby mode, comprising:
a plurality of bit line pairs;
a precharge circuit capable of precharging the bit line pairs to a voltage that is half a line voltage;
a plurality of word lines;
a row decoder that selectively activates the word lines; and
a timing control circuit that activates the precharge circuit during a predetermined period in the standby mode before the word lines are activated, and deactivates the precharge circuit in a period other than the predetermined period.

[c2] 2. The dynamic semiconductor memory device according to Claim 1, includes:
a voltage generator circuit capable of generating a voltage that is half the line voltage.

[c3] 3. The dynamic semiconductor memory device according to Claim 2, wherein the precharge circuit includes:
a first switching element connected between paired bit lines of each of the bit line pairs;

a second switching element connected between an output end of the voltage generator circuit and one of the paired bit lines; and
a third switching element connected between the output end of the voltage generator circuit and the other of the paired bit lines.

[c4] 4. The dynamic semiconductor memory device according to Claim 3, wherein the timing control circuit turns the second and third switching elements on during the predetermined period and turns them off during a period other than the predetermined period.

[c5] 5. The dynamic semiconductor memory device according to Claim 3, wherein the timing control circuit turns the first switching element on after the word lines are deactivated, and turns off the first switching element before the word lines are activated.

[c6] 6. The dynamic semiconductor memory device according to Claim 3, includes:
a voltage generator circuit for generating a voltage that is half the line voltage;
a sense amplifier for amplifying a potential difference between the paired bit lines; and
a dummy word line disposed along the word lines.

[c7] 7. The dynamic semiconductor memory device according to Claim 6, wherein:
the row decode activates the dummy word line after the word lines are deactivated but before the predetermined period; and
the timing control circuit turns the first switching element on during the predetermined period, turns the second and third switching elements off during the standby mode, and activates the sense amplifier while the dummy word line is being activated.

[c8] 8. The dynamic semiconductor memory device according to Claim 3, includes:
a voltage generator circuit for generating a voltage that is half the line voltage; and
a sense amplifier for amplifying a potential difference between the paired bit lines.

[c9] 9. The dynamic semiconductor memory device according to Claim 8, wherein:
the timing control circuit turns the first switching element on during the predetermined period, turns the second and third switching elements off during the standby mode, and activates the sense amplifier after the word lines are deactivated but before the predetermined period.

[c10] 10. The dynamic semiconductor memory device according to Claim 3, wherein:
the timing control circuit turns the first switching element on during the predetermined period, and turns the second and third switching elements on after the word lines are deactivated but before the predetermined period.

[c11] 11. The dynamic semiconductor memory device according to Claim 3, wherein:
the row decoder successively activates the plurality of word lines in order in the standby mode; and
the timing control circuit turns the first switching element on during the predetermined period each time the word lines are activated, and turns the second and third switching elements on before first activation of the word lines prior to the predetermined period.

[c12] 12. A bit line precharge method in a dynamic semiconductor memory device performing a refresh operation in a standby mode, comprising the following steps:
precharging a bit line pair to a voltage that is half a line voltage during a predetermined period in the standby mode before a word line is activated; and
electrically floating the bit line pair during a period other than the predetermined period.

[c13] 13. The bit line precharge method in a dynamic semiconductor memory device according to Claim 12, wherein the step for precharging further includes:
temporarily connecting one of the paired bit lines to a power source;
temporarily connecting the other of the paired bit lines to ground; and
short-circuiting the one and the other of the paired bit lines with each other after the paired bit lines are disconnected from the power source and the ground.

[c14] 14. A bitline precharge method in a dynamic semiconductor memory device performing a refresh operation in a standby mode, comprising the following:
providing a plurality of bit line pairs to access a plurality of columns of the memory device;
providing a precharge circuit capable of precharging the bit line pairs to a voltage that is half a line voltage;
providing a plurality of word lines to access a plurality of rows of the memory device;
providing a row decoder that selectively activates the word lines;
coupling a first switching element between paired bit lines of each of the bit line pairs;
coupling a second switching element between an output end of a voltage generator circuit and one of the paired

bit lines;

coupling a third switching element between the output end of the voltage generator circuit and the other of the paired bit lines; and

providing a timing control circuit that activates the precharge circuit during a predetermined period in the standby mode before the word lines are activated, and deactivates the precharge circuit in a period other than the predetermined period.

[c15] 15. The bitline precharge method of claim 14, wherein the timing control circuit turns the second and third switching elements on during the predetermined period and turns them off during a period other than the predetermined period.

[c16] 16. The bitline precharge method of claim 14, wherein the timing control circuit turns the first switching element on after the word lines are deactivated, and turns off the first switching element before the word lines are activated.

[c17] 17. The bitline precharge method of claim 14, wherein the timing control circuit turns the first switching element on during the predetermined period, turns the second and third switching elements off during the standby mode, and activates the sense amplifier after the word

lines are deactivated but before the predetermined period.

[c18] 18. The bitline precharge method of claim 14, wherein the timing control circuit turns the first switching element on during the predetermined period, and turns the second and third switching elements on after the word lines are deactivated but before the predetermined period.

[c19] 19. The bitline precharge method of claim 14, wherein the row decoder successively activates the plurality of word lines in order in the standby mode; and
the timing control circuit turns the first switching element on during the predetermined period each time the word lines are activated, and turns the second and third switching elements on before first activation of the word lines prior to the predetermined period.